Release 14.7 - xst P.20131013 (nt64)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Reading design: OFDM\_Top.prj

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "OFDM\_Top.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "OFDM\_Top"

Output Format : NGC

Target Device : xc3s500e-4-vq100

---- Source Options

Top Module Name : OFDM\_Top

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 24

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

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\* HDL Compilation \*

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Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/Multiplier.v" in library work

Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/Butterfly.v" in library work

Module <Multiplier> compiled

Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/EightPointsFFT.v" in library work

Module <Butterfly> compiled

Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/S2P\_REG.v" in library work

Module <EightPointsFFT> compiled

Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/S2P.v" in library work

Module <S2P\_REG> compiled

Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/QAM\_16.v" in library work

Module <S2P> compiled

Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/EightPointIFFT\_Top.v" in library work

Module <QAM\_16> compiled

Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/CPI.v" in library work

Module <EightPointIFFT\_Top> compiled

Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/Controller.v" in library work

Module <CPI> compiled

Compiling verilog file "../../../Graduation Project''/OFDM Final 8-Points/Test complete.v" in library work

Module <Controller> compiled

Module <OFDM\_Top> compiled

No errors in compilation

Analysis of file <"OFDM\_Top.prj"> succeeded.

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\* Design Hierarchy Analysis \*

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Analyzing hierarchy for module <OFDM\_Top> in library <work>.

Analyzing hierarchy for module <Controller> in library <work> with parameters.

CPIState = "00000000000000000000000000000011"

IFFTState = "00000000000000000000000000000010"

QAMState = "00000000000000000000000000000001"

S2PStateL1 = "00000000000000000000000000000001"

S2PStateL2 = "00000000000000000000000000000000"

S2P\_REGState = "00000000000000000000000000000010"

idleState = "00000000000000000000000000000000"

test = "00000000000000000000000000001010"

Analyzing hierarchy for module <S2P> in library <work> with parameters.

counterWidth = "00000000000000000000000000000010"

outPortWidth = "00000000000000000000000000000100"

Analyzing hierarchy for module <QAM\_16> in library <work> with parameters.

inPortWidth = "00000000000000000000000000000100"

outPortWidth = "00000000000000000000000000010000"

Analyzing hierarchy for module <S2P\_REG> in library <work> with parameters.

counterWidth = "00000000000000000000000000000100"

portWidth = "00000000000000000000000000010000"

registerDepth = "00000000000000000000000000001000"

Analyzing hierarchy for module <EightPointIFFT\_Top> in library <work> with parameters.

portWidth = "00000000000000000000000000010000"

Analyzing hierarchy for module <CPI> in library <work>.

Analyzing hierarchy for module <EightPointsFFT> in library <work> with parameters.

W0i = "0000000000000000"

W0r = "0000100000000000"

W1i = "1111110011110010"

W1r = "0000011101100100"

W2i = "1111101001011000"

W2r = "0000010110101000"

W3i = "1111100010001110"

W3r = "0000001100001110"

W4i = "1111100000000000"

W4r = "0000000000000000"

W5i = "1111100010001110"

W5r = "1111110011110010"

W6i = "1111101001011000"

W6r = "1111101001011000"

W7i = "0111111001111001"

W7r = "0111110001000111"

inWidth = "00000000000000000000000000010000"

Analyzing hierarchy for module <Butterfly> in library <work> with parameters.

portWidth = "00000000000000000000000000010000"

Analyzing hierarchy for module <Multiplier> in library <work> with parameters.

portWidth = "00000000000000000000000000010000"

tempWidth = "00000000000000000000000000100000"

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\* HDL Analysis \*

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Analyzing top module <OFDM\_Top>.

Module <OFDM\_Top> is correct for synthesis.

Analyzing module <Controller> in library <work>.

CPIState = 32'sb00000000000000000000000000000011

IFFTState = 32'sb00000000000000000000000000000010

QAMState = 32'sb00000000000000000000000000000001

S2PStateL1 = 32'sb00000000000000000000000000000001

S2PStateL2 = 32'sb00000000000000000000000000000000

S2P\_REGState = 32'sb00000000000000000000000000000010

idleState = 32'sb00000000000000000000000000000000

test = 32'sb00000000000000000000000000001010

Module <Controller> is correct for synthesis.

Analyzing module <S2P> in library <work>.

counterWidth = 32'sb00000000000000000000000000000010

outPortWidth = 32'sb00000000000000000000000000000100

Module <S2P> is correct for synthesis.

Analyzing module <QAM\_16> in library <work>.

inPortWidth = 32'sb00000000000000000000000000000100

outPortWidth = 32'sb00000000000000000000000000010000

Module <QAM\_16> is correct for synthesis.

Analyzing module <S2P\_REG> in library <work>.

counterWidth = 32'sb00000000000000000000000000000100

portWidth = 32'sb00000000000000000000000000010000

registerDepth = 32'sb00000000000000000000000000001000

Module <S2P\_REG> is correct for synthesis.

Analyzing module <EightPointIFFT\_Top> in library <work>.

portWidth = 32'sb00000000000000000000000000010000

Module <EightPointIFFT\_Top> is correct for synthesis.

Analyzing module <EightPointsFFT> in library <work>.

W0i = 16'sb0000000000000000

W0r = 16'sb0000100000000000

W1i = 16'sb1111110011110010

W1r = 16'sb0000011101100100

W2i = 16'sb1111101001011000

W2r = 16'sb0000010110101000

W3i = 16'sb1111100010001110

W3r = 16'sb0000001100001110

W4i = 16'sb1111100000000000

W4r = 16'sb0000000000000000

W5i = 16'sb1111100010001110

W5r = 16'sb1111110011110010

W6i = 16'sb1111101001011000

W6r = 16'sb1111101001011000

W7i = 16'sb0111111001111001

W7r = 16'sb0111110001000111

inWidth = 32'sb00000000000000000000000000010000

Module <EightPointsFFT> is correct for synthesis.

Analyzing module <Butterfly> in library <work>.

portWidth = 32'sb00000000000000000000000000010000

Module <Butterfly> is correct for synthesis.

Analyzing module <Multiplier> in library <work>.

portWidth = 32'sb00000000000000000000000000010000

tempWidth = 32'sb00000000000000000000000000100000

Module <Multiplier> is correct for synthesis.

Analyzing module <CPI> in library <work>.

INFO:Xst:1433 - Contents of array <$COND\_2> may be accessed with an index that exceeds the array size. This could cause simulation mismatch.

Module <CPI> is correct for synthesis.

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\* HDL Synthesis \*

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Performing bidirectional port resolution...

INFO:Xst:2679 - Register <i> in unit <S2P\_REG> has a constant value of 1000 during circuit operation. The register is replaced by logic.

INFO:Xst:2679 - Register <j> in unit <S2P\_REG> has a constant value of 1000 during circuit operation. The register is replaced by logic.

INFO:Xst:2679 - Register <i> in unit <CPI> has a constant value of 1001 during circuit operation. The register is replaced by logic.

Synthesizing Unit <Controller>.

Related source file is "../../../Graduation Project''/OFDM Final 8-Points/Controller.v".

Found finite state machine <FSM\_0> for signal <stateL1>.

-----------------------------------------------------------------------

| States | 4 |

| Transitions | 11 |

| Inputs | 7 |

| Outputs | 4 |

| Clock | clk (rising\_edge) |

| Reset | rst (negative) |

| Reset type | asynchronous |

| Reset State | 0000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found finite state machine <FSM\_1> for signal <stateL2>.

-----------------------------------------------------------------------

| States | 3 |

| Transitions | 12 |

| Inputs | 4 |

| Outputs | 3 |

| Clock | clk (rising\_edge) |

| Reset | rst (negative) |

| Reset type | asynchronous |

| Reset State | 0000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found 1-bit register for signal <CPIdataValid>.

Found 1-bit register for signal <CPI\_start>.

Found 1-bit register for signal <busy>.

Found 1-bit register for signal <S2P\_REG\_start>.

Found 1-bit register for signal <S2P\_start>.

Summary:

inferred 2 Finite State Machine(s).

inferred 5 D-type flip-flop(s).

Unit <Controller> synthesized.

Synthesizing Unit <S2P>.

Related source file is "../../../Graduation Project''/OFDM Final 8-Points/S2P.v".

Found 4-bit register for signal <parallelOut>.

Found 1-bit register for signal <done>.

Found 1-bit register for signal <convDone>.

Found 3-bit up counter for signal <counter>.

Found 4-bit register for signal <tempReg>.

Summary:

inferred 1 Counter(s).

inferred 10 D-type flip-flop(s).

Unit <S2P> synthesized.

Synthesizing Unit <QAM\_16>.

Related source file is "../../../Graduation Project''/OFDM Final 8-Points/QAM\_16.v".

Found 16x32-bit ROM for signal <in$rom0000>.

Found 16-bit register for signal <outI>.

Found 16-bit register for signal <outR>.

Summary:

inferred 1 ROM(s).

inferred 32 D-type flip-flop(s).

Unit <QAM\_16> synthesized.

Synthesizing Unit <S2P\_REG>.

Related source file is "../../../Graduation Project''/OFDM Final 8-Points/S2P\_REG.v".

Found 16-bit register for signal <out0I>.

Found 16-bit register for signal <out1I>.

Found 16-bit register for signal <out0R>.

Found 16-bit register for signal <out2I>.

Found 16-bit register for signal <out1R>.

Found 16-bit register for signal <out3I>.

Found 16-bit register for signal <out2R>.

Found 16-bit register for signal <out4I>.

Found 16-bit register for signal <out3R>.

Found 16-bit register for signal <out5I>.

Found 16-bit register for signal <out4R>.

Found 16-bit register for signal <out6I>.

Found 16-bit register for signal <out5R>.

Found 16-bit register for signal <out7I>.

Found 16-bit register for signal <out6R>.

Found 16-bit register for signal <out7R>.

Found 1-bit register for signal <done>.

Found 5-bit up counter for signal <count>.

Found 128-bit register for signal <dataI>.

Found 128-bit register for signal <dataR>.

Found 1-bit register for signal <ready>.

Summary:

inferred 1 Counter(s).

inferred 514 D-type flip-flop(s).

Unit <S2P\_REG> synthesized.

Synthesizing Unit <CPI>.

Related source file is "../../../Graduation Project''/OFDM Final 8-Points/CPI.v".

Register <frame<8>> equivalent to <frame<0>> has been removed

Found 1-bit register for signal <done>.

Found 1-bit register for signal <serialOut>.

Found 1-bit register for signal <outValid>.

Found 1-bit 32-to-1 multiplexer for signal <$varindex0000> created at line 66.

Found 7-bit up counter for signal <count>.

Found 256-bit register for signal <frame<0:7>>.

Found 6-bit up counter for signal <regCount>.

INFO:Xst:738 - HDL ADVISOR - 256 flip-flops were inferred for signal <frame>. You may be trying to describe a RAM in a way that is incompatible with block and distributed RAM resources available on Xilinx devices, or with a specific template that is not supported. Please review the Xilinx resources documentation and the XST user manual for coding guidelines. Taking advantage of RAM resources will lead to improved device usage and reduced synthesis time.

Summary:

inferred 2 Counter(s).

inferred 259 D-type flip-flop(s).

inferred 33 Multiplexer(s).

Unit <CPI> synthesized.

Synthesizing Unit <Butterfly>.

Related source file is "../../../Graduation Project''/OFDM Final 8-Points/Butterfly.v".

Found 16-bit adder for signal <bflyOut1I>.

Found 16-bit subtractor for signal <bflyOut2I>.

Found 16-bit subtractor for signal <bflyOut1R>.

Found 16-bit adder for signal <bflyOut2R>.

Found 16-bit adder for signal <bflyOut1I$addsub0000> created at line 61.

Found 16-bit adder for signal <bflyOut1R$addsub0000> created at line 60.

Found 16-bit subtractor for signal <bflyOut2I$addsub0000> created at line 63.

Found 16-bit subtractor for signal <bflyOut2R$addsub0000> created at line 62.

Summary:

inferred 8 Adder/Subtractor(s).

Unit <Butterfly> synthesized.

Synthesizing Unit <EightPointsFFT>.

Related source file is "../../../Graduation Project''/OFDM Final 8-Points/EightPointsFFT.v".

Found 16-bit register for signal <out0I>.

Found 16-bit register for signal <out1I>.

Found 16-bit register for signal <out0R>.

Found 16-bit register for signal <out2I>.

Found 16-bit register for signal <out1R>.

Found 16-bit register for signal <out3I>.

Found 16-bit register for signal <out2R>.

Found 16-bit register for signal <out4I>.

Found 16-bit register for signal <out3R>.

Found 16-bit register for signal <out5I>.

Found 16-bit register for signal <out4R>.

Found 16-bit register for signal <out6I>.

Found 16-bit register for signal <out5R>.

Found 16-bit register for signal <out7I>.

Found 16-bit register for signal <out6R>.

Found 16-bit register for signal <out7R>.

Summary:

inferred 256 D-type flip-flop(s).

Unit <EightPointsFFT> synthesized.

Synthesizing Unit <EightPointIFFT\_Top>.

Related source file is "../../../Graduation Project''/OFDM Final 8-Points/EightPointIFFT\_Top.v".

Found 16-bit register for signal <IFFTout0I>.

Found 16-bit register for signal <IFFTout1I>.

Found 16-bit register for signal <IFFTout0R>.

Found 16-bit register for signal <IFFTout2I>.

Found 16-bit register for signal <IFFTout1R>.

Found 16-bit register for signal <IFFTout3I>.

Found 16-bit register for signal <IFFTout2R>.

Found 16-bit register for signal <IFFTout4I>.

Found 16-bit register for signal <IFFTout3R>.

Found 16-bit register for signal <IFFTout5I>.

Found 16-bit register for signal <IFFTout4R>.

Found 16-bit register for signal <IFFTout6I>.

Found 16-bit register for signal <IFFTout5R>.

Found 16-bit register for signal <IFFTout7I>.

Found 16-bit register for signal <IFFTout6R>.

Found 16-bit register for signal <IFFTout7R>.

Found 16-bit adder for signal <FFTin0I>.

Found 16-bit adder for signal <FFTin1I>.

Found 16-bit adder for signal <FFTin2I>.

Found 16-bit adder for signal <FFTin3I>.

Found 16-bit adder for signal <FFTin4I>.

Found 16-bit adder for signal <FFTin5I>.

Found 16-bit adder for signal <FFTin6I>.

Found 16-bit adder for signal <FFTin7I>.

Found 16-bit adder for signal <negFFTOut0I>.

Found 16-bit adder for signal <negFFTOut1I>.

Found 16-bit adder for signal <negFFTOut2I>.

Found 16-bit adder for signal <negFFTOut3I>.

Found 16-bit adder for signal <negFFTOut4I>.

Found 16-bit adder for signal <negFFTOut5I>.

Found 16-bit adder for signal <negFFTOut6I>.

Found 16-bit adder for signal <negFFTOut7I>.

Summary:

inferred 256 D-type flip-flop(s).

inferred 16 Adder/Subtractor(s).

Unit <EightPointIFFT\_Top> synthesized.

Synthesizing Unit <OFDM\_Top>.

Related source file is "../../../Graduation Project''/OFDM Final 8-Points/Test complete.v".

Unit <OFDM\_Top> synthesized.

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HDL Synthesis Report

Macro Statistics

# ROMs : 1

16x32-bit ROM : 1

# Multipliers : 48

16x16-bit multiplier : 48

# Adders/Subtractors : 112

16-bit adder : 64

16-bit subtractor : 48

# Counters : 4

3-bit up counter : 1

5-bit up counter : 1

6-bit up counter : 1

7-bit up counter : 1

# Registers : 88

1-bit register : 12

16-bit register : 66

32-bit register : 8

4-bit register : 2

# Multiplexers : 2

1-bit 32-to-1 multiplexer : 1

32-bit 9-to-1 multiplexer : 1

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\* Advanced HDL Synthesis \*

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Analyzing FSM <FSM\_1> for best encoding.

Optimizing FSM <U0/stateL2/FSM> on signal <stateL2[1:2]> with sequential encoding.

-------------------

State | Encoding

-------------------

0000 | 00

0001 | 01

0010 | 10

-------------------

Analyzing FSM <FSM\_0> for best encoding.

Optimizing FSM <U0/stateL1/FSM> on signal <stateL1[1:2]> with gray encoding.

-------------------

State | Encoding

-------------------

0000 | 00

0001 | 01

0010 | 11

0011 | 10

-------------------

INFO:Xst:2261 - The FF/Latch <IFFTout3R\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout3R\_13> <IFFTout3R\_14> <IFFTout3R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout5I\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout5I\_13> <IFFTout5I\_14> <IFFTout5I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout0I\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout0I\_13> <IFFTout0I\_14> <IFFTout0I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout4R\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout4R\_13> <IFFTout4R\_14> <IFFTout4R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout6I\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout6I\_13> <IFFTout6I\_14> <IFFTout6I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout1I\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout1I\_13> <IFFTout1I\_14> <IFFTout1I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout5R\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout5R\_13> <IFFTout5R\_14> <IFFTout5R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout7I\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout7I\_13> <IFFTout7I\_14> <IFFTout7I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout0R\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout0R\_13> <IFFTout0R\_14> <IFFTout0R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout2I\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout2I\_13> <IFFTout2I\_14> <IFFTout2I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout6R\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout6R\_13> <IFFTout6R\_14> <IFFTout6R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout1R\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout1R\_13> <IFFTout1R\_14> <IFFTout1R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout3I\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout3I\_13> <IFFTout3I\_14> <IFFTout3I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout7R\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout7R\_13> <IFFTout7R\_14> <IFFTout7R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout2R\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout2R\_13> <IFFTout2R\_14> <IFFTout2R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout4I\_12> in Unit <U4> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout4I\_13> <IFFTout4I\_14> <IFFTout4I\_15>

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Advanced HDL Synthesis Report

Macro Statistics

# FSMs : 2

# ROMs : 1

16x32-bit ROM : 1

# Multipliers : 48

16x16-bit multiplier : 48

# Adders/Subtractors : 112

16-bit adder : 64

16-bit subtractor : 48

# Counters : 4

3-bit up counter : 1

5-bit up counter : 1

6-bit up counter : 1

7-bit up counter : 1

# Registers : 1332

Flip-Flops : 1332

# Multiplexers : 2

1-bit 32-to-1 multiplexer : 1

32-bit 9-to-1 multiplexer : 1

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\* Low Level Synthesis \*

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INFO:Xst:2261 - The FF/Latch <IFFTout3R\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout3R\_13> <IFFTout3R\_14> <IFFTout3R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout5I\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout5I\_13> <IFFTout5I\_14> <IFFTout5I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout0I\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout0I\_13> <IFFTout0I\_14> <IFFTout0I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout4R\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout4R\_13> <IFFTout4R\_14> <IFFTout4R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout6I\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout6I\_13> <IFFTout6I\_14> <IFFTout6I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout1I\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout1I\_13> <IFFTout1I\_14> <IFFTout1I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout5R\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout5R\_13> <IFFTout5R\_14> <IFFTout5R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout7I\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout7I\_13> <IFFTout7I\_14> <IFFTout7I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout0R\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout0R\_13> <IFFTout0R\_14> <IFFTout0R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout2I\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout2I\_13> <IFFTout2I\_14> <IFFTout2I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout6R\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout6R\_13> <IFFTout6R\_14> <IFFTout6R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout1R\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout1R\_13> <IFFTout1R\_14> <IFFTout1R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout3I\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout3I\_13> <IFFTout3I\_14> <IFFTout3I\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout7R\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout7R\_13> <IFFTout7R\_14> <IFFTout7R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout2R\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout2R\_13> <IFFTout2R\_14> <IFFTout2R\_15>

INFO:Xst:2261 - The FF/Latch <IFFTout4I\_12> in Unit <EightPointIFFT\_Top> is equivalent to the following 3 FFs/Latches, which will be removed : <IFFTout4I\_13> <IFFTout4I\_14>

Optimizing unit <OFDM\_Top> ...

Optimizing unit <Controller> ...

Optimizing unit <S2P> ...

Optimizing unit <QAM\_16> ...

Optimizing unit <S2P\_REG> ...

Optimizing unit <CPI> ...

Optimizing unit <Butterfly> ...

Optimizing unit <EightPointsFFT> ...

Optimizing unit <EightPointIFFT\_Top> ...

Final Macro Processing ...

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Final Register Report

Macro Statistics

# Registers : 723

Flip-Flops : 723

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : OFDM\_Top.ngr

Top Level Output File Name : OFDM\_Top

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 7

Cell Usage :

# BELS : 9842

# GND : 1

# INV : 704

# LUT1 : 913

# LUT2 : 1552

# LUT3 : 217

# LUT4 : 107

# MUXCY : 2865

# MUXF5 : 86

# MUXF6 : 40

# MUXF7 : 4

# MUXF8 : 2

# VCC : 1

# XORCY : 3350

# FlipFlops/Latches : 723

# FDC : 427

# FDCE : 291

# FDR : 1

# FDRE : 4

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 6

# IBUF : 3

# OBUF : 3

# MULTs : 12

# MULT18X18SIO : 12

=========================================================================

Device utilization summary:

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Selected Device : 3s500evq100-4

Number of Slices: 1996 out of 4656 42%

Number of Slice Flip Flops: 723 out of 9312 7%

Number of 4 input LUTs: 3493 out of 9312 37%

Number of IOs: 7

Number of bonded IOBs: 7 out of 66 10%

Number of MULT18X18SIOs: 12 out of 20 60%

Number of GCLKs: 1 out of 24 4%

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 723 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

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------------------------------------------+------------------------+-------+

Control Signal | Buffer(FF name) | Load |

------------------------------------------+------------------------+-------+

U5/rst\_inv1\_INV\_0\_1(U5/rst\_inv1\_INV\_0\_1:O)| NONE(U4/U0/out2I\_3) | 361 |

U0/rst\_inv(U5/rst\_inv1\_INV\_0:O) | NONE(U0/CPI\_start) | 357 |

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Timing Summary:

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Speed Grade: -4

Minimum period: 46.229ns (Maximum Frequency: 21.631MHz)

Minimum input arrival time before clock: 4.646ns

Maximum output required time after clock: 4.310ns

Maximum combinational path delay: No path found

Timing Detail:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'

Clock period: 46.229ns (frequency: 21.631MHz)

Total number of paths / destination ports: 14486403148241 / 1017

-------------------------------------------------------------------------

Delay: 46.229ns (Levels of Logic = 54)

Source: U3/out7I\_11 (FF)

Destination: U4/U0/out5I\_15 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: U3/out7I\_11 to U4/U0/out5I\_15

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FDCE:C->Q 2 0.591 0.447 U3/out7I\_11 (U3/out7I\_11)

MULT18X18SIO:B11->P11 2 4.654 0.447 U4/U0/s14/Multiplier\_U1/Mmult\_\_old\_temp\_1 (U4/U0/s14/Madd\_bflyOut1R\_addsub0000\_lut<0>)

INV:I->O 1 0.704 0.000 U4/U0/s14/Msub\_bflyOut2R\_addsub0000\_lut<0>1\_INV\_0 (U4/U0/s14/Msub\_bflyOut2R\_addsub0000\_lut<0>)

MUXCY:S->O 1 0.464 0.000 U4/U0/s14/Msub\_bflyOut2R\_addsub0000\_cy<0> (U4/U0/s14/Msub\_bflyOut2R\_addsub0000\_cy<0>)

MUXCY:CI->O 1 0.059 0.000 U4/U0/s14/Msub\_bflyOut2R\_addsub0000\_cy<1> (U4/U0/s14/Msub\_bflyOut2R\_addsub0000\_cy<1>)

XORCY:CI->O 1 0.804 0.595 U4/U0/s14/Msub\_bflyOut2R\_addsub0000\_xor<2> (U4/U0/s14/Madd\_bflyOut2R\_lut<2>)

LUT1:I0->O 1 0.704 0.000 U4/U0/s14/Madd\_bflyOut2R\_cy<2>\_rt (U4/U0/s14/Madd\_bflyOut2R\_cy<2>\_rt)

MUXCY:S->O 1 0.464 0.000 U4/U0/s14/Madd\_bflyOut2R\_cy<2> (U4/U0/s14/Madd\_bflyOut2R\_cy<2>)

XORCY:CI->O 6 0.804 0.844 U4/U0/s14/Madd\_bflyOut2R\_xor<3> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd2\_lut<5>)

LUT1:I0->O 1 0.704 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd2\_cy<5>\_rt (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd2\_cy<5>\_rt)

MUXCY:S->O 1 0.464 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd2\_cy<5> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd2\_cy<5>)

XORCY:CI->O 1 0.804 0.595 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd2\_xor<6> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd8\_lut<8>)

LUT1:I0->O 1 0.704 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd8\_cy<8>\_rt (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd8\_cy<8>\_rt)

MUXCY:S->O 1 0.464 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd8\_cy<8> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd8\_cy<8>)

MUXCY:CI->O 1 0.059 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd8\_cy<9> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd8\_cy<9>)

XORCY:CI->O 1 0.804 0.595 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd8\_xor<10> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_lut<14>)

LUT1:I0->O 1 0.704 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_cy<14>\_rt (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_cy<14>\_rt)

MUXCY:S->O 1 0.464 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_cy<14> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_cy<14>)

MUXCY:CI->O 1 0.059 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_cy<15> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_cy<15>)

MUXCY:CI->O 1 0.059 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_cy<16> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_cy<16>)

XORCY:CI->O 1 0.804 0.499 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd12\_xor<17> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd\_2011)

LUT2:I1->O 1 0.704 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd14\_lut<20> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd14\_lut<20>)

MUXCY:S->O 1 0.464 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd14\_cy<20> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd14\_cy<20>)

XORCY:CI->O 1 0.804 0.499 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd14\_xor<21> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd\_2118)

LUT2:I1->O 1 0.704 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd15\_lut<21> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd15\_lut<21>)

MUXCY:S->O 1 0.464 0.000 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd15\_cy<21> (U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd15\_cy<21>)

XORCY:CI->O 3 0.804 0.610 U4/U0/s24/Multiplier\_U4/Mmult\_\_old\_temp\_1\_Madd15\_xor<22> (U4/U0/s24/mul4<11>)

LUT2:I1->O 1 0.704 0.455 U4/U0/s24/Madd\_bflyOut1IC101 (U4/U0/s24/Madd\_bflyOut1IC10)

LUT3:I2->O 1 0.704 0.000 U4/U0/s24/Madd\_bflyOut1I\_Madd\_lut<12> (U4/U0/s24/Madd\_bflyOut1I\_Madd\_lut<12>)

MUXCY:S->O 1 0.464 0.000 U4/U0/s24/Madd\_bflyOut1I\_Madd\_cy<12> (U4/U0/s24/Madd\_bflyOut1I\_Madd\_cy<12>)

XORCY:CI->O 12 0.804 1.136 U4/U0/s24/Madd\_bflyOut1I\_Madd\_xor<13> (U4/U0/s32/Multiplier\_U2/Mmult\_\_old\_temp\_1\_Madd7\_lut<16>)

LUT1:I0->O 1 0.704 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<16>\_rt (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<16>\_rt)

MUXCY:S->O 1 0.464 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<16> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<16>)

MUXCY:CI->O 1 0.059 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<17> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<17>)

MUXCY:CI->O 1 0.059 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<18> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<18>)

MUXCY:CI->O 1 0.059 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<19> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_cy<19>)

XORCY:CI->O 1 0.804 0.499 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd7\_xor<20> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd\_206)

LUT2:I1->O 1 0.704 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd10\_lut<20> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd10\_lut<20>)

MUXCY:S->O 1 0.464 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd10\_cy<20> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd10\_cy<20>)

XORCY:CI->O 1 0.804 0.499 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd10\_xor<21> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd\_2114)

LUT2:I1->O 1 0.704 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd13\_lut<21> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd13\_lut<21>)

MUXCY:S->O 1 0.464 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd13\_cy<21> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd13\_cy<21>)

XORCY:CI->O 1 0.804 0.499 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd13\_xor<22> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd\_2213)

LUT2:I1->O 1 0.704 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd14\_lut<22> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd14\_lut<22>)

MUXCY:S->O 1 0.464 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd14\_cy<22> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd14\_cy<22>)

XORCY:CI->O 1 0.804 0.595 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd14\_xor<23> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd15\_lut<23>)

LUT1:I0->O 1 0.704 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd15\_cy<23>\_rt (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd15\_cy<23>\_rt)

MUXCY:S->O 1 0.464 0.000 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd15\_cy<23> (U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd15\_cy<23>)

XORCY:CI->O 4 0.804 0.666 U4/U0/s32/Multiplier\_U3/Mmult\_\_old\_temp\_1\_Madd15\_xor<24> (U4/U0/s32/mul3<13>)

LUT2:I1->O 1 0.704 0.000 U4/U0/s32/Msub\_bflyOut2I\_addsub0000\_lut<13> (U4/U0/s32/Msub\_bflyOut2I\_addsub0000\_lut<13>)

MUXCY:S->O 1 0.464 0.000 U4/U0/s32/Msub\_bflyOut2I\_addsub0000\_cy<13> (U4/U0/s32/Msub\_bflyOut2I\_addsub0000\_cy<13>)

XORCY:CI->O 1 0.804 0.499 U4/U0/s32/Msub\_bflyOut2I\_addsub0000\_xor<14> (U4/U0/s32/bflyOut2I\_addsub0000<14>)

LUT2:I1->O 1 0.704 0.000 U4/U0/s32/Msub\_bflyOut2I\_lut<14> (U4/U0/s32/Msub\_bflyOut2I\_lut<14>)

MUXCY:S->O 0 0.464 0.000 U4/U0/s32/Msub\_bflyOut2I\_cy<14> (U4/U0/s32/Msub\_bflyOut2I\_cy<14>)

XORCY:CI->O 1 0.804 0.000 U4/U0/s32/Msub\_bflyOut2I\_xor<15> (U4/U0/stage3Out5I<15>)

FDC:D 0.308 U4/U0/out5I\_15

----------------------------------------

Total 46.229ns (36.250ns logic, 9.979ns route)

(78.4% logic, 21.6% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 9 / 8

-------------------------------------------------------------------------

Offset: 4.646ns (Levels of Logic = 2)

Source: rst (PAD)

Destination: U1/parallelOut\_3 (FF)

Destination Clock: clk rising

Data Path: rst to U1/parallelOut\_3

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 2 1.218 0.447 rst\_IBUF (rst\_IBUF)

INV:I->O 361 0.704 1.366 U5/rst\_inv1\_INV\_0 (U0/rst\_inv)

FDRE:R 0.911 U1/parallelOut\_0

----------------------------------------

Total 4.646ns (2.833ns logic, 1.813ns route)

(61.0% logic, 39.0% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 3 / 3

-------------------------------------------------------------------------

Offset: 4.310ns (Levels of Logic = 1)

Source: U0/busy (FF)

Destination: busy (PAD)

Source Clock: clk rising

Data Path: U0/busy to busy

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 2 0.591 0.447 U0/busy (U0/busy)

OBUF:I->O 3.272 busy\_OBUF (busy)

----------------------------------------

Total 4.310ns (3.863ns logic, 0.447ns route)

(89.6% logic, 10.4% route)

=========================================================================

Total REAL time to Xst completion: 28.00 secs

Total CPU time to Xst completion: 27.94 secs

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Total memory usage is 4744116 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 498 ( 0 filtered)

Number of infos : 104 ( 0 filtered)